# Integrated Power Transistor in 0.18-$\mu$m CMOS Technology for RF System-on-Chip Applications

Heng-Ming Hsu, Jiong-Guang Su, Chih-Wei Chen, Denny D. Tang, Chun Hsiung Chen, and Jack Yuan-Chen Sun

***Abstract*—A novel design and performance of a power MOS transistor for RF system-on-chip applications are reported. The power MOS transistor with high breakdown voltage is integrated into 0.18-$\mu$m CMOS technology with only one additional mask. By an optimized design considering all aspects of dc and RF performances, a power MOS transistor with 16-GHz cutoff frequency and 24-GHz maximum oscillation frequency has been demonstrated. In addition, the power gain is 12 dB at 2.4 GHz with power-added efficiency of 50%. In this study, the device architectures that include drain engineering, substrate engineering, and gate scaling are investigated comprehensively.**

***Index Terms*—0.18-$\mu$m CMOS, RF power MOS transistor, system-on-chip (SoC).**

## I. Introduction

THE progress of RF CMOS technology has enabled highly integrated communication devices, such as handset and portable electronic appliances. Passive elements such as inductors, metal–insulator–metal (MIM) capacitors, and varactors are successfully integrated into 0.18-$\mu$m CMOS technology to provide system-on-chip (SoC) solutions for RF systems [1]. However, power transistors have not been integrated into state-of-the-art technologies. Silicon power transistors are the most obvious choice for CMOS integration due to their process compatibility. In addition, silicon integrated power amplifiers [2], [3] are inherently superior in terms of cost, compact size, and short time-to-market. Hence, the development of suitable power transistors for SoC is indispensable.

The design of a power MOS transistor with high breakdown voltage is the most important issue. Deep-submicrometer technologies adopt thinner gate oxide and shallower source/drain junction and may face challenges in embedding a power MOS transistor due to the inherently low breakdown voltages associated with the resulting devices. In this study, only one additional mask is used to implement an integrated power MOS transistor with a breakdown voltage greater than 8 V. Both dc and RF performances of the power MOS transistor will be investigated under the adjustment of layout parameters. All of the parameters will affect the intrinsic behaviors of MOS transistor, such as drain resistance, substrate resistance, and gate scaling.

For the consideration of mass production, the threshold voltage stability, gate oxide integrity, and hot carrier effect of the power MOS transistor are examined in order to provide excellent qualified components. Based on the proposed novel device, successful implementation of a power MOS transistor in 0.18-$\mu$m CMOS technology is demonstrated for mass production of RF integrated circuits (ICs) integrating power amplifiers.

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H.-M. Hsu and C. H. Chen are with the Department of Electrical Engineering, National Taiwan University, Taipei 106, Taiwan, R.O.C.

J.-G. Su, C.-W. Chen, D. D. Tang, and J. Y.-C. Sun are with the Research Development Center, Taiwan Semiconductor Manufacturing Company, Hsinchu 300, Taiwan, R.O.C. (e-mail: hunming_hsu@tsmc.com.tw).

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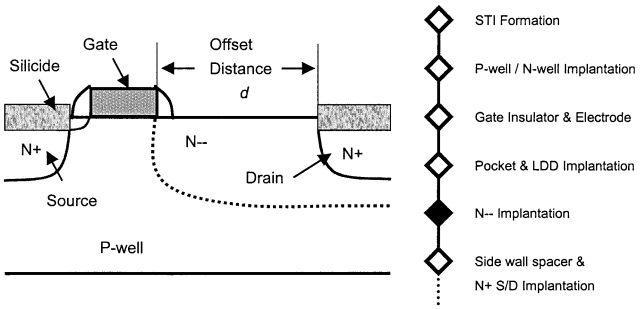



Fig. 1. Brief process flow and cross section of the power MOS transistor.

## II. Device Fabrication and Design

The fabrication of the power MOS transistor is based on 0.18-$\mu$m CMOS technology, with an additional N$-$ implantation before the N$+$ source/drain implantation. The dosages of N$-$ and N$+$ are $10^{14}$ cm$^{-2}$ and $10^{16}$ cm$^{-2}$, respectively. The lower dosage of N$-$ implantation reduces the electric field near the drain side and therefore increases the breakdown voltage. A brief process flow and cross section of the n-type power MOS transistor are illustrated in Fig. 1, the offset distance ($d$), N$+$ edge to poly edge on the drain side, is varied to investigate its influence on the power MOS transistor.

In addition, a patterned oxide film on N$-$ area was used for avoiding the silicide formation on this area. A counterpart without patterned oxide film was also fabricated for comparison. The avoiding of silicide (or called nonsilicide) is beneficial to improve the breakdown voltage of drain side. However, additional N$-$ implantation and patterned oxide film tend to increase the in-series drain resistance and thus degrade the RF performances of the power MOS transistor. Therefore, the "drain engineering" is essential to achieve high breakdown voltage and excellent RF performances.

For high-power transmission, a larger gatewidth is usually used for increasing the gate transconductance and driving capability. To reduce the gate resistance, the finger-gated type is adopted as depicted in Fig. 2 [4]. However, the increase of finger number tends to increase the substrate resistance and is more likely to trigger snapback and reduce the breakdown voltage [5]. To reduce the substrate resistance, the p-well

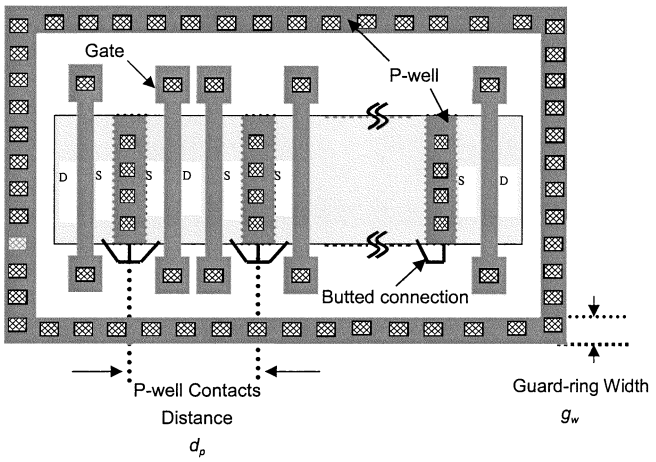



Fig. 2. Layout of the power MOS transistor.

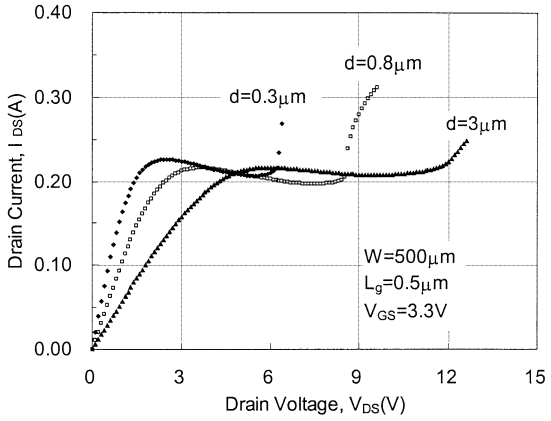



Fig. 3. $I_{\rm DS}$-$V_{\rm DS}$ characteristics with different offset distances.

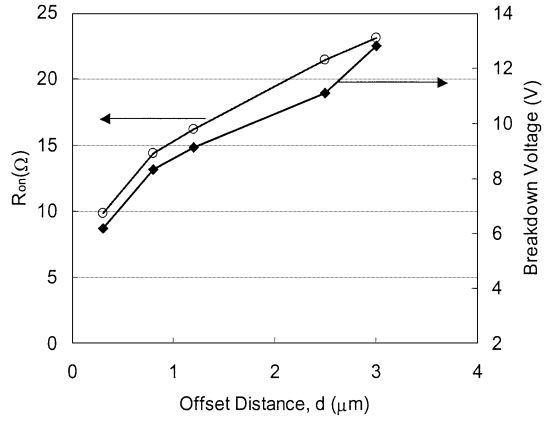



Fig. 4. Plots for on-state resistance ($R_{\rm on}$) and breakdown voltage with various offset distances.

contacts are installed on the active region, and the guard-ring is used to surround the active region as depicted in Fig. 2. These approaches are denoted as the "substrate engineering," and the corresponding effects on dc and RF characteristics of the power MOS transistor are discussed in the following sections.

## III. DC AND RF PARAMETERS

As mentioned in Section II, the parameters of layout and process that are related to the drain engineering, the offset distance ($d$), and with/without silicide, must be optimized to achieve high breakdown voltage and excellent RF figure-of-merit (FOM). In addition, the parameters related to the substrate engineering, the distance between p-well contacts on active region ($d_p$), and the guard-ring width ($g_w$) also have to be considered carefully. Specifically the characteristics involving breakdown voltage, on-state resistance ($R_{\rm on}$), cutoff frequency ($f_T$), maximum oscillator frequency ($f_{\rm MAX}$) [6], stability frequency ($f_K$) [7], power gain, 1-dB gain compression point ($P_{\rm 1dB}$), and power-added efficiency (PAE) are adopted to investigate the device performances.

To obtain the breakdown voltage, the gate voltage is operated at 3.3 V while varying the drain voltage. The on-state resistance is obtained from the slope of the linear region of drain current to voltage curve when the power MOS transistor is biased at the gate voltage with maximum gate transconductance and a small drain bias (e.g., 0.2 V) [8]. To obtain the RF performances, the power MOS transistor is biased at gate voltage with maximum gate transconductance and the drain bias is equal to 3.3 V. The values of $f_T$, $f_{\rm MAX}$, and $f_K$ are extracted from the obtained $S$-parameters in the high-frequency measurement. All the $S$-parameters are obtained from the on-wafer measurement, and the de-embedding procedure is performed to remove the undesired pads parasitics [9].

The cutoff frequency of a power MOS transistor is extracted by extrapolating the regression line of $|H_{21}|$ to the corresponding frequency value of $|H_{21}| = 1$. The maximum oscillator frequency is extracted from maximum available power gain [6]. Since the power MOS transistor is used as a power amplifier, the stability issue is critical. The stability frequency is the upper limit frequency at which the power MOS transistor is operated at potentially unstable region [7] and can be extracted from the frequency when the stability $k$ factor equals 1. The smaller $f_K$ value implies that the device tends to match stable conditions on lower frequencies [7].

The large-signal performance is measured under the condition of output power at 17 dBm and the operation frequency at 2.4 GHz. The devices are biased at 5% of saturation current (class AB), and the output signal is matching at maximum PAE. From the large-signal measurement results, the linearity index and efficiency can be obtained from the $P_{\rm 1dB}$ and PAE values, respectively.

## IV. CHARACTERISTICS OF POWER MOS TRANSISTORS

The effects of offset distance, with/without silicide on N− area, guard-ring width, p-well contacts distance, channel length, and total gatewidth on the dc and RF characteristics are discussed in the following:

### A. Effects of Offset Distance of N− Area

The $I_{\rm DS}$-$V_{\rm DS}$ characteristics for various offset distances are shown in Fig. 3. It is clear that long offset distance is beneficial to achieve higher breakdown voltage, however, it corresponds to a smaller slope of the $I_{\rm DS}$-$V_{\rm DS}$ curve that implies a higher on-state resistance ($R_{\rm on}$). The corresponding breakdown voltage and $R_{\rm on}$ are illustrated in Fig. 4. The breakdown voltage

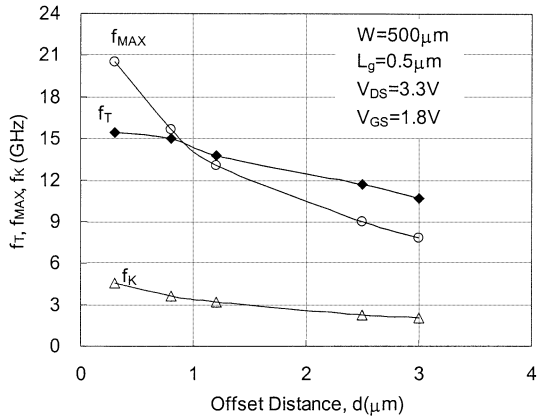
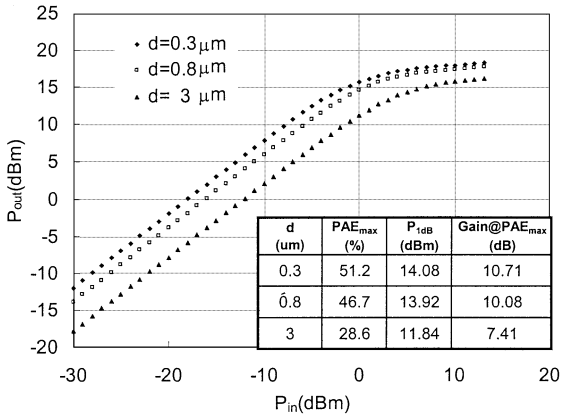



Fig. 5. Plots for cutoff frequency ($f_T$), maximum oscillation frequency ($f_{\rm MAX}$), and stability frequency ($f_K$) with various offset distances.




| d (um) | PAE$_{max}$ (%) | P$_{1dB}$ (dBm) | Gain@PAE$_{max}$ (dB) |
|---|---|---|---|
| 0.3 | 51.2 | 14.08 | 10.71 |
| 0.8 | 46.7 | 13.92 | 10.08 |
| 3 | 28.6 | 11.84 | 7.41 |

Fig. 6. Plots for large-signal performances with various offset distances.

is increased with the increase of offset distance because the increased drain resistance suppresses the electric field near the drain side. When the offset distance increases from 0.3 to 3 $\mu$m, the breakdown voltage increases from 6 to 13 V, and the on-state resistance increases from 10 to 24 $\Omega$. Therefore, a tradeoff between the on-state resistance and breakdown voltage needs to be considered carefully for obtaining the optimum performance.

The RF performances of the power MOS transistors with different offset distances are illustrated in Fig. 5. The cutoff frequency of a power MOS transistor is increased with decreased offset distance since it is proportional to the gate transconductance $g_m$ as given by

$$f_T \cong \frac{g_m}{2\pi\sqrt{C_{\rm gg}^2 - C_{\rm gd}^2}} \tag{1}$$

where $C_{\rm gg}$ is the total gate capacitance that includes the intrinsic and extrinsic gate capacitances [10], and $C_{\rm gd}$ is the gate-to-drain capacitance. As expected, a smaller offset distance results in smaller drain resistance and higher transconductance. Therefore, the cutoff frequency of a power MOS transistor is decreased from 15.5 to 10.5 GHz when the offset distance is increased from 0.3 to 3 $\mu$m.

The effect on the maximum oscillation frequency is more sensitive than the $f_T$ smaller offset distance is beneficial for obtaining high $f_{\rm MAX}$. As a result, 20.5 GHz of $f_{\rm MAX}$ is obtained when the offset distance is 0.3 $\mu$m. Equation (2) shows the effects of small-signal model on $f_{\rm MAX}$

$$\left(f_{\rm MAX} = \frac{f_T}{2\sqrt{g_{\rm sd}\left(R_g + R_s\right) + 2\pi f_T R_g C_{\rm gd}}}\right) \tag{2}$$

where $g_{\rm sd}$ is the channel conductance and $R_g$ is the gate resistance. Since the gate resistances of the testing devices are identical due to the same finger-gated structure, from measurement results, the increase of $f_{\rm MAX}$ is attributed to the increase of gate transconductance and the decrease of series resistance.

Nevertheless, a smaller offset distance is not beneficial for stable design. As observed in Fig. 5, higher $f_K$ is obtained when the offset distance is decreased. The increase of $f_K$ is attributed to the increase of $g_m$ and the reduction of drain resistance. The effects on $f_K$ under a small-signal model may be expressed as [7]

$$\left(f_K \approx f_T \cdot \frac{\dfrac{C_{\rm gd}}{C_{\rm gg}}}{\dfrac{C_{\rm gs}}{C_{\rm gg}}\sqrt{8g_{\rm ds}R_g\dfrac{C_{\rm gd}}{C_{\rm gg}}\left[g_m\dfrac{C_{\rm gs}}{C_{\rm gg}}R_g + \dfrac{C_{\rm gd}}{C_{\rm gg}}\left(3g_mR_g+1\right)\right]}}\right). \tag{3}$$

As a summary, the best choice is to specify the lower bound of breakdown voltage, which is 8 V in our investigation. Then, according to Fig. 4, the corresponding offset distance should be greater than 0.8 $\mu$m. In addition, it is observed that a smaller offset distance is helpful for $f_T$, $f_{\rm MAX}$, and $R_{\rm on}$ of the power MOS transistor. Therefore, the offset distance of 0.8 $\mu$m is the optimal condition. Since the difference in $f_K$ with an offset distance ranging from 0.8 to 3 $\mu$m is kept within 2 GHz, its effect on the stability for 0.8 $\mu$m is not significant.

The large-signal performances of output power versus input power with different offset distances are illustrated in Fig. 6; smaller offset distance produces larger output power with the input power increasing from $-30$ to 15 dBm. This behavior results from the fact that lower series resistance provides larger current flow into the output terminal and hence increases output power. The larger output power gives better linearity and efficiency, and the corresponding $P_{\rm 1dB}$, PAE, and gain are depicted in the inset of Fig. 6.

### *B. Effects of Silicide on N− Area*

As mentioned in Section II, the nonsilicide on N− area has been used to increase the breakdown voltage of power MOS transistor. The power MOS transistor with silicide on N− area exhibits smaller drain resistance than that without silicide on N− area. According to our observation, minimal degradation on the values of $f_T$, $f_{\rm MAX}$, and $f_K$ is found for the power MOS transistor either with or without silicide on the N− implantation area.

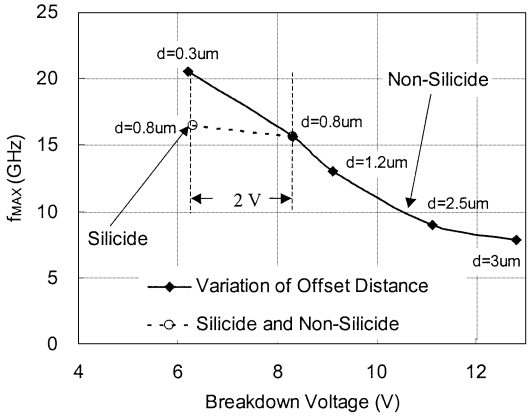



Fig. 7. Plots for maximum oscillation frequency versus breakdown voltage. Solid symbols represent the variation of offset distances, and empty symbols represent the comparison of the power MOS transistor with/without silicide.

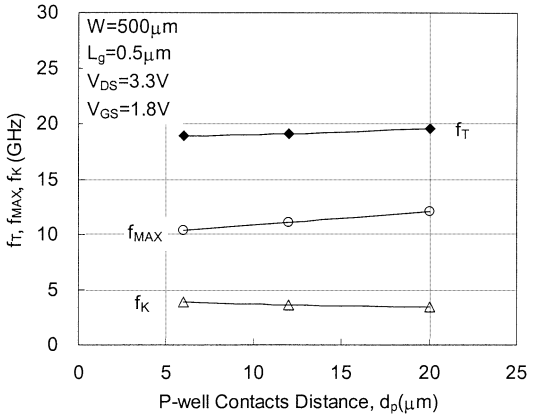



Fig. 9. Plots for cutoff frequency ($f_T$), maximum oscillation frequency ($f_{\rm MAX}$), and stability frequency ($f_K$) with different distances between p-well contacts on the active area.

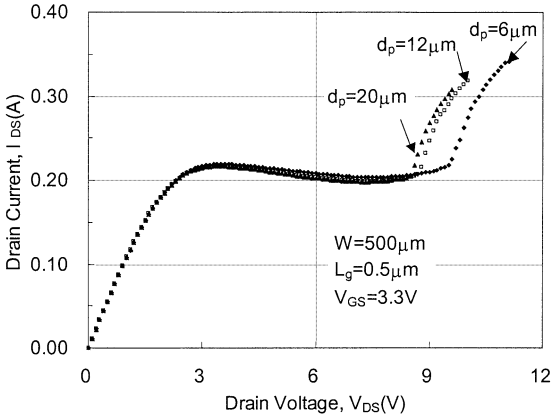
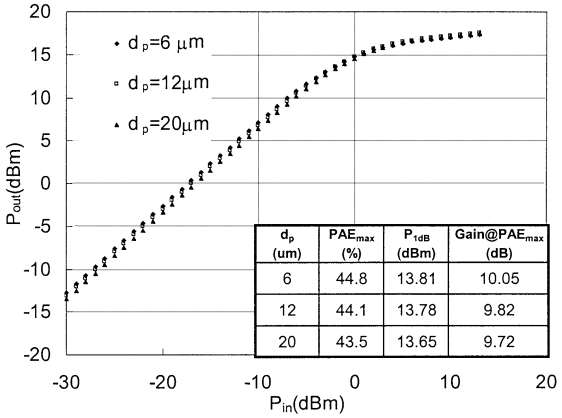



Fig. 8. $I_{\rm DS}$-$V_{\rm DS}$ characteristics with different distances between p-well contacts on the active area.




| $d_p$ (um) | $PAE_{max}$ (%) | $P_{1dB}$ (dBm) | Gain@$PAE_{max}$ (dB) |
|---|---|---|---|
| 6 | 44.8 | 13.81 | 10.05 |
| 12 | 44.1 | 13.78 | 9.82 |
| 20 | 43.5 | 13.65 | 9.72 |

Fig. 10. Plots for large-signal performances with different distances between p-well contacts on the active area.

Note that the breakdown voltage has an obvious improvement by using the nonsilicide device. The breakdown voltage can be improved either by decreasing the offset distance or avoiding the silicide on the N− area. However, as compared with the previous results of offset distance, as shown in Fig. 7, the nonsilicide device shows only a slight reduction in the value of $f_{\rm MAX}$.

With an improvement of 2-V breakdown voltage, the degradation of $f_{\rm MAX}$ with the offset distance decreasing from 0.3 to 0.8 $\mu$m is approximately 5 GHz. Nevertheless, with the identical 2-V improvement of breakdown voltage, the value of $f_{\rm MAX}$ by using nonsilicide on the N− area shows a degradation of only 0.8 GHz. The result is attributed to an increase of junction capacitance when the offset distance is increased. The increase of junction capacitance is therefore to decrease the output power of the device and thus the value of $f_{\rm MAX}$.

### C. Effects of p-Well Contact Distance

The reduction of substrate resistance suppresses more snapback effect and, thus, increases the breakdown voltage. As depicted in Fig. 2, the additional p-well contacts on the active region can decrease substrate resistance due to more current paths to silicon substrate. The decreased distance between p-well contacts ($d_p$) results in the improvement of breakdown voltage. The corresponding dc characteristics are shown in Fig. 8. As the guard-ring width is kept fixed, the power MOS transistor with smaller $d_p$(= 6 $\mu$m) exhibits higher breakdown voltage (= 10 V) because of the smaller p-well substrate resistance. The effects of guard-ring width will be addressed in the next section.

The RF performances of the power MOS transistor with various distances of $d_p$ are shown in Fig. 9. The values of $f_T$ and $f_K$ are insensitive to $d_p$, while the values of $f_{\rm MAX}$ are degraded by a value of about 2 GHz when the distances of $d_p$ are decreased from 20 to 6 $\mu$m. The reduction of $f_{\rm MAX}$ is attributed to the lower p-well substrate resistance. When the p-well substrate resistance is higher, the impedance underneath the drain junction is therefore higher. As a result, the high impedance path prevents loss of power, and more power can be delivered to the output. Fig. 10 illustrates that the large-signal behaviors with various distances of $d_p$ show no obvious discrepancy in these curves; while referring to the dc characteristics of Fig. 8, the drain current and voltage performances are almost identical before the occurrence of breakdown voltage. This means that the large-signal behaviors are similar with different p-well substrate

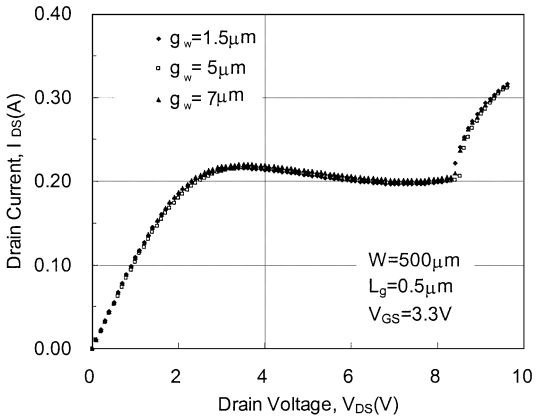



Fig. 11. $I_{\rm DS}$-$V_{\rm DS}$ characteristics with different guard-ring widths on silicon substrate.

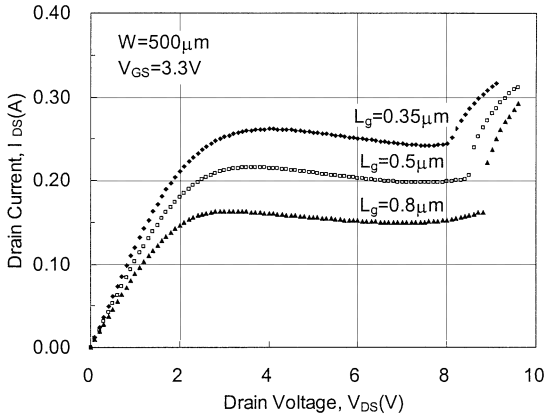



Fig. 12. $I_{\rm DS}$-$V_{\rm DS}$ characteristics with different channel lengths of the power MOS transistor.

TABLE I
LIST OF CUTOFF FREQUENCY ($f_T$), MAXIMUM OSCILLATION FREQUENCY ($f_{\rm MAX}$), AND STABILITY FREQUENCY ($f_K$) WITH VARIOUS GUARD-RING WIDTHS ON SUBSTRATE

| Guard-ring width (μm) | 1.5 | 5 | 7 |
|---|---|---|---|
| $f_T$(GHz) | 14.39 | 14.41 | 14.48 |
| $f_{MAX}$(GHz) | 16.29 | 15.64 | 15.07 |
| $f_K$(GHz) | 3.58 | 3.64 | 3.66 |

resistances. As a result, the variations in $P_{\rm 1dB}$, PAE, and gain are insensitive as depicted in the inset of Fig. 10.

### *D. Effects of Guard-Ring Width*

As illustrated in Fig. 2, the p-well contacts of the power MOS transistor were arranged as guard-ring type in order to reduce the substrate resistance and coupled noise [11]. The reduction of substrate resistance is beneficial to suppress the snapback of parasitic bipolar action. The total substrate resistance includes p-well substrate resistance and guard-ring resistance. Since the guard-ring resistance is mainly owing to the possible current crowding, the experiments considering various guard-ring widths are performed to investigate this effect. With increasing guard-ring width, the contact numbers on p-well pickup are increased, resulting in the decrease of guard-ring resistance.

The dc and RF characteristics with different guard-ring widths are illustrated in Fig. 11 and Table I, respectively. A minimal discrepancy of both dc and RF performances is observed when the guard-ring width is varied. Comparing with the p-well substrate resistance, the influences on guard-ring resistance are minor. Hence, the p-well substrate resistance on the active region should be controlled to be as small as possible to provide high breakdown voltage.

### *E. Effects of Gate Scaling*

The channel length $L_g$ of the power MOS transistor in this study is mainly chosen to be 0.5 $\mu$m. The effects of channel length are investigated using three different values of $L_g$, i.e., 0.35, 0.5, and 0.8 $\mu$m. Figs. 12 and 13 show the dc and RF characteristics of the power MOS transistors, respectively. Accompanied with a decrease of channel length, the breakdown voltage

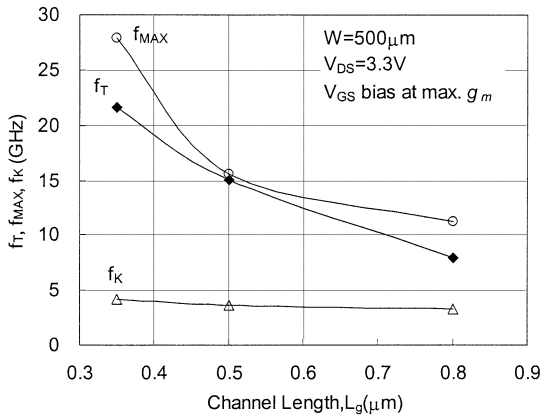
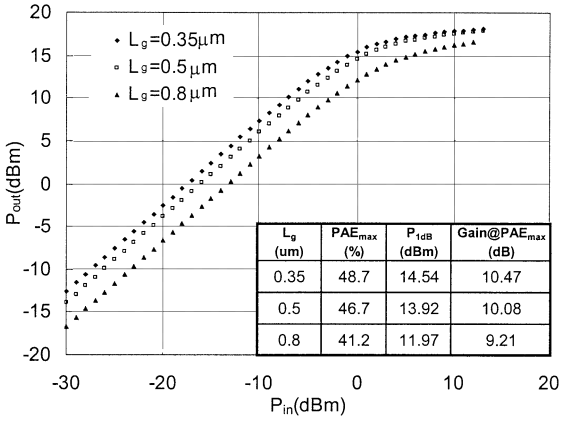



Fig. 13. Plots for cutoff frequency ($f_T$), maximum oscillation frequency ($f_{\rm MAX}$), and stability frequency ($f_K$) with various channel lengths.

is reduced, and the cutoff frequency and $f_{\rm MAX}$ are increased. High $f_{\rm MAX}$ of 28 GHz is obtained when the channel length is scaled down to 0.35 $\mu$m, and yet, the corresponding gate resistance is increased, implying lower breakdown voltage and inferior stability [12]. Therefore, in the sense of breakdown voltage, a 0.5-$\mu$m channel length is more suitable for high-power operation.

The large-signal performances for different channel lengths are illustrated in Fig. 14; smaller channel length results in larger output power. This high output power capability owes to the larger transconductance of the device [13]. Note that the smaller channel length device has larger output power capability, i.e., more output power can be delivered under the same input power as shown in Fig. 14. Hence, better linearity and efficiency can be obtained. The values of $P_{\rm 1dB}$, PAE, and gain are depicted in the inset of Fig. 14.

The dc characteristics of power MOS transistors with channel length of 0.5 $\mu$m and various gatewidths are shown in Fig. 15. It is found that the breakdown voltage is almost independent of the gatewidth and all power MOS transistors have a breakdown voltage higher than 8 V. In addition, the self-heating effect is stronger when the gatewidth is increased. A comparison of RF characteristics is shown in Fig. 16. The cutoff frequency and $f_{\rm MAX}$ of the power MOS transistors are degraded with in-




| $L_g$ (um) | $PAE_{max}$ (%) | $P_{1dB}$ (dBm) | Gain@$PAE_{max}$ (dB) |
|---|---|---|---|
| 0.35 | 48.7 | 14.54 | 10.47 |
| 0.5 | 46.7 | 13.92 | 10.08 |
| 0.8 | 41.2 | 11.97 | 9.21 |

Fig. 14. Plots for large-signal performances with various channel lengths.

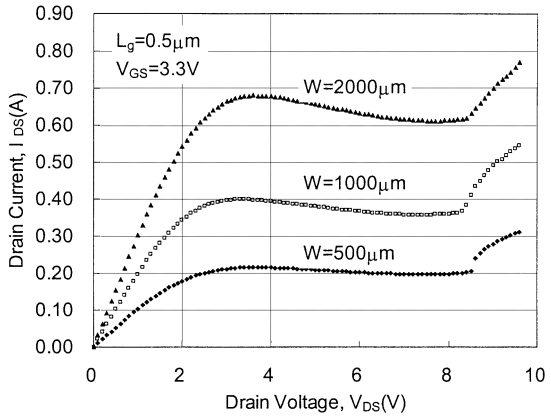



Fig. 15. $I_{\rm DS}$-$V_{\rm DS}$ characteristics with different gatewidths of the power MOS transistor.

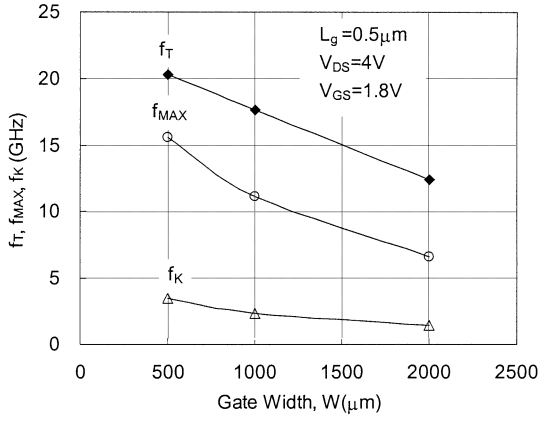



Fig. 16. Plots for cutoff frequency ($f_T$), maximum oscillation frequency ($f_{\rm MAX}$), and stability frequency ($f_K$) with various gatewidths.

creasing gatewidth. The degradation of bandwidth is due to the reduced normalized gate transconductance which is caused by the thermal heating of the channel. Therefore, to achieve high $f_T$ and $f_{\rm MAX}$, the gatewidth of 500 $\mu$m is adopted for further investigations. Lastly, the power MOS transistor with smaller gatewidth has a higher value of $f_K$, which implies that the power MOS transistor with smaller gatewidth is unstable. The high $f_K$ is attributed to a reduction of gate resistance. Nevertheless, the

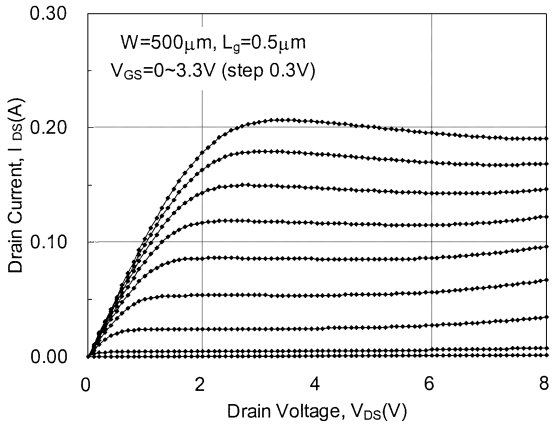



Fig. 17. $I_{\rm DS}$-$V_{\rm DS}$ characteristics of the designed power MOS transistor.

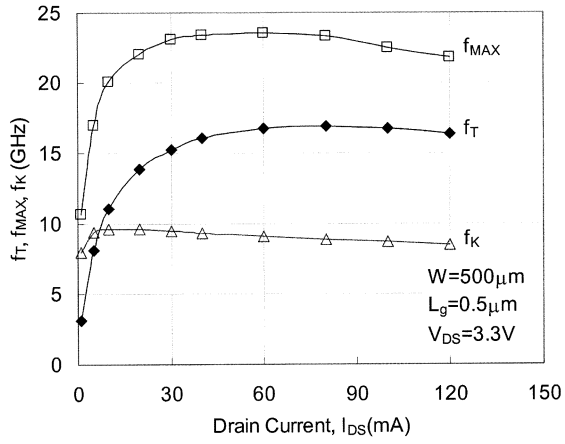



Fig. 18. Plots for cutoff frequency ($f_T$), maximum oscillation frequency ($f_{\rm MAX}$), and stability frequency ($f_K$) of the designed power MOS transistor.

difference of $f_K$ is restricted within 2 GHz and, hence, the stability of power MOS transistor with small gatewidth remains acceptable.

### *F. Design of Power MOS Transistors*

From Sections IV-A–IV-E, the power MOS transistor can acquire satisfactory characteristics with the following designs based on 0.8-$\mu$m offset distance, nonsilicide on N$-$ area, and 5-$\mu$m guard-ring width of the p-well pickup. According to the investigation in Section IV-C, smaller $d_p$ is beneficial for higher breakdown voltage. Therefore, the best performance results from a design such that the p-well contacts should be connected to the source contacts on active region (i.e., butted structure). From these layout parameters, the dc and RF characteristics of the power MOS transistor with a channel length of 0.5 $\mu$m and a gatewidth of 500 $\mu$m are shown in Figs. 17 and 18. The observed breakdown voltages are greater than 8 V, the maximum $f_T$ and $f_{\rm MAX}$ are 16 and 24 GHz, respectively, and the minimum $f_K$ is 8.5 GHz.

As shown in Fig. 19, the output power is greater than 17 dBm, the 1-dB gain compression point is at 12.5 dBm, and the third-order intermodulation point is at 22.3 dBm. The corresponding power gain and PAE are depicted in Fig. 20 with output power ranging from $-$10 to 17.5 dBm. It is found that the PAE of the

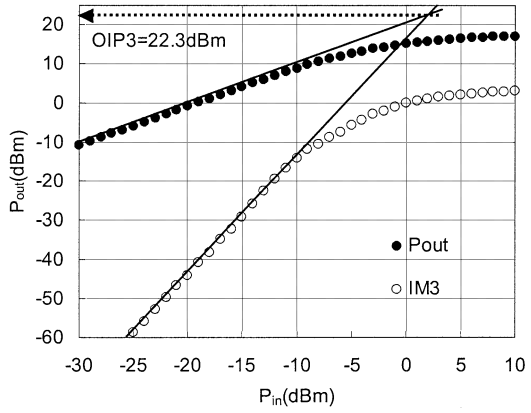



Fig. 19. Plots for output and input powers. The power MOS transistor is biased at $Vd = 3.3$ V, $Vg = 1.1$ V (5% of Isat), and has output matching at $\mathrm{PAE}_{\max}$, with an operation frequency at 2.4 GHz.

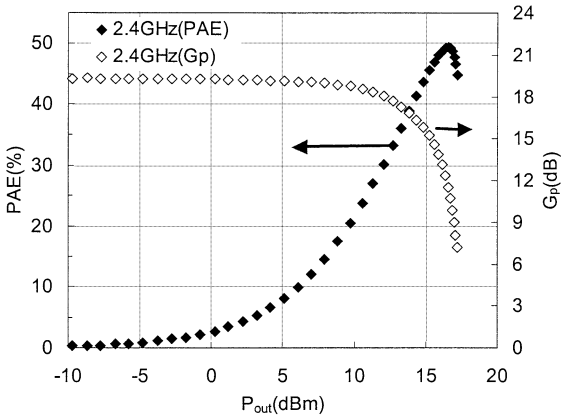



Fig. 20. Plots for output power, PAE, and power gain of the designed power MOS transistor. The dc is biased at $Vd = 3.3$ V, $Vg = 1.1$ V(5% of Isat), and has output matching at $\mathrm{PAE}_{\max}$, with an operation frequency at 2.4 GHz.

power MOS transistor reaches a value of 50% at an output power of 16 dBm, which meets with the specifications of Bluetooth, wireless LAN, and Personal Handy-phone System applications. All the results show that the designed power MOS transistor with high linearity and power gain can be implemented into wireless portable ICs.

Table II shows a comparison of the results on this study with those previously reported in the literature [14]–[16]. With a smaller total gatewidth $W$ ($= 500$ $\mu$m), our results of $f_T$, $f_{\mathrm{MAX}}$, and PAE are comparable to those with larger $W$, and our design provides a better power gain. In addition, this work can provide an integrated power device in 0.18-$\mu$m CMOS technology for a single-chip solution.

## V. Qualification Results

The device reliability is essential to the qualification of a power MOS transistor. The qualification items involve threshold voltage stability, gate oxide integrity, and hot carrier effect. The threshold voltage stability using $V_{\mathrm{DS}} = 3.6$ V stress on 125 °C after 168 h is shown in Table III, and the fluctuations of 12 samples are all within 1.29%. The gate oxide integrity is measured under $V_{\mathrm{DS}} = 6.8$ V, 7.0 V, and 7.2 V at 125 °C as shown in Fig. 21. The $V_{\mathrm{DS}}$ values are normalized to 3.6 V by using the Weibull probability model [17], and it is found that the gate oxide lifetime is greater than $10^5$ h (about 11.5 years). Here, only the dc stress result is addressed, not considering the

TABLE II
Comparison of Reported Power MOS Transistors

| References | 1995 [14] | 1998 [15] | 2000 [16] | This Study |
|---|---|---|---|---|
| W($\mu$m) | 1600 | 7500 | 800 | 500 |
| Freq.(GHz) | 0.9 | 1.9 | 2 | 2.4 |
| $V_{DS}$(Voltage) | 3.5 | 3 | 3 | 3.3 |
| $f_{MAX}$(GHz) | 6 | 4 | 19 | 24 |
| $f_T$(GHz) | 8.3 | 8 | 25 | 16 |
| $P_{out}$(dBm) | 23.9 | 24.8 | 21 | 16 |
| Gain(dB) | 12 | 7.5 | 16 | 20 |
| $PAE_{max}$(%) | 55 | 50 | 50 | 50 |
| Gain@ $PAE_{max}$(dB) | 8 | 7.5 | 8 | 12 |
| Integrated Technology | -- | -- | -- | **0.18μm CMOS** |

TABLE III
Threshold Voltage ($V_t$) Test for the Designed Power MOS Transistor

| | Initial Results | Results with 168 Hours Burn-in | | |
|---|---|---|---|---|
| Die No. | $V_t$ (V) | $V_t$(V) | Shift Voltage (V) | Shift Rate (%) |
| 1 | 0.634 | 0.639 | 0.005 | 0.789 |
| 2 | 0.655 | 0.660 | 0.005 | 0.763 |
| 3 | 0.633 | 0.636 | 0.003 | 0.474 |
| 4 | 0.672 | 0.674 | 0.002 | 0.298 |
| 5 | 0.710 | 0.712 | 0.002 | 0.282 |
| 6 | 0.715 | 0.718 | 0.003 | 0.420 |
| 7 | 0.699 | 0.701 | 0.002 | 0.286 |
| 8 | 0.695 | 0.704 | 0.009 | 1.295 |
| 9 | 0.677 | 0.682 | 0.005 | 0.739 |
| 10 | 0.709 | 0.717 | 0.008 | 1.128 |
| 11 | 0.713 | 0.722 | 0.009 | 1.262 |
| 12 | 0.700 | 0.706 | 0.006 | 0.857 |
| 13 | 0.695 | 0.697 | 0.002 | 0.288 |
| | | Max. $V_t$ Shift | 0.009 | 1.295 |

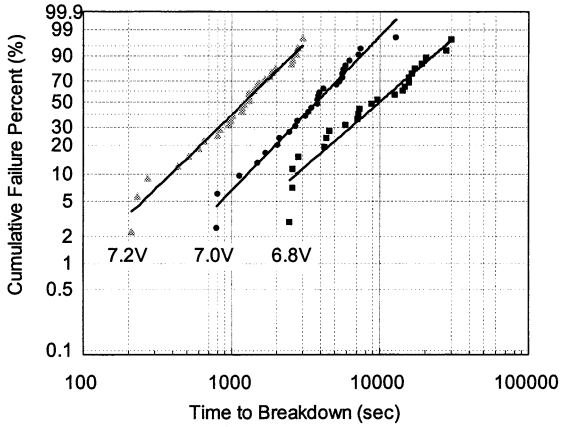



Fig. 21. Oxide integrity test for the designed power MOS transistor.

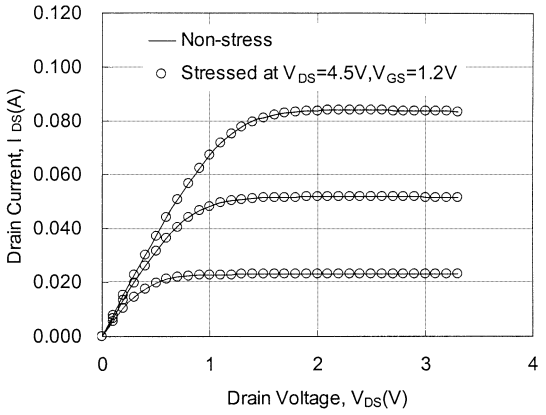



Fig. 22. Hot carrier effect test for the designed power MOS transistor.

large-signal stress on this item. The large-signal stress algorithm is another reliability topic of interest and is not included in this paper.

The stress results of hot carrier effect are shown in Fig. 22, which indicates that the drain currents vary from 85.686 to 85.629 mA after 40 000 s of stress when the drain voltage is biased at 4.5 V. The drain current degrades by only 0.066% after 40 000 s of stressing; it is predicted that the same degradation is achieved under normal bias (e.g., 3.3 V) conditions for 8.937 years [18]. All the qualification items have three lots of results and show excellent reliability on the power MOS transistor in 0.18-$\mu$m CMOS technology.

## VI. Conclusion

A complete portfolio of the RF power MOS transistor integrated into 0.18-$\mu$m CMOS has been successfully demonstrated. The effects on N$-$ area with/without silicide, offset distance on drain side, substrate resistance, scaled channel length, and gatewidth on dc and RF performances have been addressed in this paper. The higher breakdown voltage has been achieved by using additional N$-$ implantation with an offset at drain side, nonsilicide formation on this area, and the butted connection structure. The RF performances such as $f_T$ of 16 GHz, $f_{\mathrm{MAX}}$ of 24 GHz, power gain of 12 dB, and nearly 50% PAE with class AB bias point at 2.4 GHz have been achieved with this designed power MOS transistor.

To guarantee the reliability of power MOS devices, complete qualifications on threshold voltage stability, gate oxide integrity, and hot carrier effect have been examined experimentally. The results promise not only excellent performances, but also the robustness for the mass production of power MOS transistors. Finally, the development of the RF power MOS transistor in this study may be instrumental to perspective integrating design of all short-range, low-power, and high-frequency application components in a single chip.

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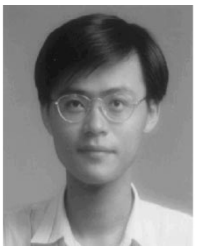

**Heng-Ming Hsu** received the M.S. degree from the National Taiwan University, Taipei, Taiwan, R.O.C.

After serving in the Chinese Airforce Army, he joined the RF devices development project of the Taiwan Semiconductor Manufacturing Company (TSMC), Hsinchu, Taiwan, R.O.C., in 1997, where he was engaged in the research of bulk silicon RF CMOS integrated devices, involving active devices (RF CMOS and power devices) and passive devices such as high-$Q$ inductors, MIM capacitors, interconnections, and so on. He holds four R.O.C patents and one U.S. patent in the field of RF devices. His current interests are RF device optimization engineering and process module development.

**Jiong-Guang Su** was born in Keelung, Taiwan, R.O.C., in 1972. He received the Ph.D. degree in electronics from the National Chiao-Tung University, Hsinchu, Taiwan, R.O.C., in 2002.

In October 1996, he joined the research project on deep submicrometer CMOS technology and physics with ERSO and was involved with PMOS design and modeling. In June of 1998, he participated in the research project in static and RF modeling of CMOS and BJT devices in the Device and Reliability Division, Winbond Electronic Company Ltd. From 2000 to 2002, he joined the Mixed-Signal/RF Project of the Taiwan Semiconductor Manufacture Company (TSMC). Hsinchu, Taiwan, R.O.C. He currently serves on the Ministry of National Defense, R.O.C. He has experience on a variety of RF integrated devices, including CMOS, BJTs, power MOSs, inductors, varactors, and substrate coupling with an emphasis on characterization and modeling. His continuing interests are the design of CMOS RFICs and wireless power sources.

**Chih-Wei Chen**, photograph and biography not available at the time of publication.

**Denny D. Tang**, photograph and biography not available at the time of publication.

**Chun Hsiung Chen**, photograph and biography not available at the time of publication.

**Jack Yuan-Chen Sun**, photograph and biography not available at the time of publication.